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BSCpE 3A

**BCD Down Counter**

**VHDL Code:**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.NUMERIC\_STD.ALL; -- Better than STD\_LOGIC\_ARITH/UNSIGNED

entity bcddowncounter1 is

Port (

clk : in STD\_LOGIC;

rst : in STD\_LOGIC; -- Active-low reset

q : out STD\_LOGIC\_VECTOR (3 downto 0)

);

end bcddowncounter1;

architecture Behavioral of bcddowncounter1 is

constant MAX\_COUNT : integer := 50\_000\_000 - 1; -- For 1 sec @ 50 MHz

signal counter : unsigned(25 downto 0) := (others => '0');

signal clkd : std\_logic := '0';

signal q\_reg : unsigned(3 downto 0) := "1001"; -- Start at 9 (BCD)

begin

-- Clock Divider to generate 1 Hz from 50 MHz

process(clk)

begin

if rising\_edge(clk) then

if counter = MAX\_COUNT then

counter <= (others => '0'); -- Reset counter

clkd <= not clkd; -- Toggle every 1 sec

else

counter <= counter + 1;

end if;

end if;

end process;

-- BCD Down Counter Logic

process(clkd, rst)

begin

if rst = '0' then

q\_reg <= "1001"; -- Reset to 9

elsif falling\_edge(clkd) then

if q\_reg = "0000" then

q\_reg <= "1001"; -- Wrap around after 0

else

q\_reg <= q\_reg - 1;

end if;

end if;

end process;

-- Assign output

q <= not std\_logic\_vector(q\_reg);

end Behavioral;